AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A method for customization of a FPGA-based SoC design, the method comprising:

selecting a system design component used for customizing the FPGA-based SoC design;

configuring said selected system design component with parameters for use with the FPGA-based SoC design;

said selected system component sending said parameters used to configure said selected system design component to peer system design components; [[and]]

configuring said peer system design components using said sent parameters during customization of the FPGA-based SoC design; and

generating hardware description language code from the selected system design components and peer system design components.

2. (Cancelled)

3. (Currently Amended) The method according to claim 1 [[2]], further comprising the step of propagating said parameter used to configure said peer system design component to subsequently selected system design components used to configure the FPGA-based SoC design.

4. (Original) The method according to claim 1, wherein said selecting step further comprises the step of providing an option for selecting an implementation selected from the group consisting of a hardware implementation and a software implementation.

5. (Original) The method according to claim 1, wherein said step of selecting said system component further comprises selecting a system component from the group consisting of a hardware core and a software core.

6. (Currently amended) The method according to claim 1, wherein the method further comprises the step of initializing only the selected system design components that are utilized for customizing the FPGA-based SoC design.

7. (Currently amended) A machine readable storage having stored thereon, a computer program having a plurality of code sections, said code sections executable by a machine for causing the machine to perform the steps of:

selecting a system design component used for customizing a FPGA-based SoC;

configuring said selected system component with parameters for use with said FPGA-based SoC;

said selected system component sending said parameters used to configure said selected system component to peer system components; [[and]]

configuring said peer system components using said sent parameters during customization of said FPGA-based SoC; and

generating hardware description language code from the selected system design components and peer system design components.

8. (Cancelled)

9. (Currently Amended) The machine readable storage according to claim 7 [[8]], further comprising sections of code for causing the machine to propagate said parameter used to configure said peer system component to subsequently selected system design components used to configure said FPGA-based SoC design.

Claims 10-18 (Cancelled)

19. (New) A method for creating a design of a field programmable gate array-based (FPGA-based) system on chip (SoC), comprising:

selecting hardware design components from a library in response to user input to a design tool executing on a processor;

associating at least one parameter value with a first selected hardware design component in response to user input to the design tool;

automatically associating by the design tool, without user specification of the association, the at least one parameter value with a second selected hardware design component; and

generating by the design tool hardware description language code from the first and second hardware design components using the at least one parameter value.

20. (New) The method of claim 19, further comprising outputting from the design tool data that indicate respective numbers of FPGA resources used by each selected design component in response to user input.

21. (New) The method of claim 19, further comprising:

selecting a software design component from a library in response to user input to the design tool;

automatically associating by the design tool, without user specification of the association, the at least one parameter value with the software design component; and

generating by the design tool a header file for the software design component using the at least one parameter value.

22. (New) The method of claim 21, further comprising:

associating at least one parameter value with a third hardware design component in response to user input to the design tool;

associating at least one parameter value with a fourth hardware design component in response to user input to the design tool;

checking by the design tool for inconsistency between the least one parameter value of the third hardware design component and the at least one parameter value of a fourth hardware design component; and

outputting by the design tool to a user data that indicates each parameter inconsistency.

23. (New) An apparatus for creating a design of a field programmable gate array-based (FPGA-based) system on chip (SoC), comprising:

means for selecting hardware design components from a library in response to user input to a design tool executing on a processor;

means for associating at least one parameter value with a first hardware design component in response to user input to the design tool;

means for automatically associating by the design tool, without user specification of the association, the at least one parameter value with a second hardware design component; and

means for generating by the design tool hardware description language code from the first and second hardware design components using the at least one parameter value.

24. (New) A system for creating a design of a field programmable gate array-based (FPGA-based) system on chip (SoC), comprising:

a selector module adapted to select, responsive to user input, components from a library of hardware design components and software design components;

a customizer module coupled to the selector module, the customizer module adapted to relate, responsive to user input, parameter values with the selected components, and for at least one parameter value related by a user to a first one of the selected components automatically relate the at least one parameter value to a second one of the selected components without user specification of the relation to the second one of the components;

an analyzer module coupled to the customizer module and adapted to check for inconsistency of parameter values between the selected components; and

a code generator coupled to the customizer module and adapted to generate hardware description language code from the selected components and related parameter values.